Docket No.: 4363P004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	)	
	)	
Arash Hassibi, et al.	)	Examiner: Quang D. Vu
	)	
Application No: 09/843,486	)	Art Unit: 2811
	)	
Filed: April 25, 2001	)	
	)	
For: OPTIMAL SIMULTANEOUS DESIGN AND FLOORPLANNING OF INTEGRATED CIRCUIT	)	

Commissioner for Patents
.P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Request for Continuation. It is respectfully requested that the cited information be considered and that the enclosed copy of the PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 10/29/03

Robert B. O'Rourke, Reg. No. 46,972

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(408) 720-8300

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Janece Shannon — 10/29/2003
10-29-03

Janece Shannon — ***Date***

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet	1	of	1

Complete if Known	
Application Number	09/843,486
Filing Date	April 25, 2001
First Named Inventor	Arash Hassibi
Art Unit	2811
Examiner Name	Quang D. Vu
Attorney Docket Number	4363P004

Examiner Initials*	Cite No.[1]	INFORMATION	T[2]
		"A public use of the claimed invention that can be attributed to the inventorship entity was held in June of 2000".	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

ARASH HASSIBI, ET AL.

Application No.: 09/843,486

Filed: April 25, 2001

For: **Optimal Simultaneous Design and Floorplanning of Integrated Circuit**

Art Group: 2811

Examiner: Quang D. Vu

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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The references were cited in a Search Report dated September 24, 2003 (copy enclosed herewith) in a counterpart PCT application.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

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Janece Shannon — *10-29-03*

Janece Shannon — *Date*

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Application Number	09/843,486
Filing Date	April 25, 2001
First Named Inventor	Arash Hassibi
Art Unit	2811
Examiner Name	Quang D. Vu
Attorney Docket Number	4363P004

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		HERSHENSON M DELM ET AL: **"Optimal Design Of A CMOS OP-AMP Via Geometric Programming", IEEE Transactions On Computer-Aided Design Of Integrated Circuits and Systems**, January 2001, IEEE Vol. 20, No. 1, Pages 1-21, Paragraph '007A', Table 1.	
		BALASA, F:, "**Modeling Non-Slicing Floorplans With Binary Trees**", 2000 IEEE/ACM International Conference On Computer-Aided Design. ICCAD-2000. San Jose, CA, Nov. 5-9, 2000, IEEE/ACM International Conference On Computer-Aided Design, New York, NY, IEEE, Nov. 5, 2000, Pages 13-16.	

Examiner Signature		Date Considered	

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